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- https://www.du.ac.in/uploads/new-web/15092023_Indis_sem1.pdf
- https://www.du.ac.in/uploads/new-web/notifications-2021/28032023_nep-Faculty%20of%20Interdisciplinary%20&%20Applied%20Sciences.pdf
- https://www.du.ac.in/uploads/new-web/15092023_Indis_sem3.pdf
- https://www.du.ac.in/uploads/new-web/18092023_Inter_4.pdf

DISCIPLINE SPECIFIC ELECTIVES (DSE-2)

CREDIT DISTRIBUTION, ELIGIBILITY AND PRE-REQUISITES OF THE COURSE

Course title & Code	Credits	Credit distribution of the course			Eligibility criteria	Pre-requisite of the course (if any)
		Lecture	Tutorial	Practical/Practice		
Advance Computer System Architecture	4	3	-	1	Class XII passed with Physics + Mathematics/Applied Mathematics + Chemistry OR Physics + Mathematics/Applied Mathematics + Computer Science/Informatics Practices	Microprocessor (DSC 11, Sem IV) or equivalent to Computer System Architecture, Operating system(DSE 2B, Sem IV)

Learning Objectives

- To give the students an elaborate idea about the different memory systems and buses.
- To introduce the advanced processor architectures to the students.
- To make the students know about the importance of multiprocessor and multicompiler.
- To study about data flow computer architectures
- To make students know about the Parallelism concepts

Learning outcomes

The Learning Outcomes of this course are as follows:

- Demonstrate concepts of parallelism in hardware/software.
- Discuss memory organization and mapping techniques.
- Describe architectural features of advanced processors.
- Interpret performance of different pipelined processors.
- Explain data flow in arithmetic algorithms
- Development of software to solve computationally intensive problems.

SYLLABUS OF ELDSE-4B

Total Hours- Theory: 45 Hours, Practicals: 30 Hours

UNIT – I (10 Hours)

Computer Architecture & Organization: Instruction codes, Computer instructions, Basics of Input/Output & Interrupts, Complete computer description & design of basic

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computer. Control Unit: Hardwired vs. Micro programmed control unit. Flynn's classification.

UNIT – II (11 Hours)

Memory Hierarchy: Hierarchical memory organization, Types of Cache Memory, Memory Interleaving, Replacement algorithms + write policy, Concept of Virtual Memory and Virtual Machine.

Parallel Processing: Definition, Theory of Parallelism. Parallel Computer Models, Implicit Parallelism vs. explicit parallelism, Levels of parallelism. Software Parallelism, Hardware Parallelism.

UNIT – III (12 Hours)

Pipelining: Basic Concepts of pipelining, Linear pipeline processor, Asynchronous and Synchronous models, speed up, Efficiency, Throughput, Instruction pipeline. Pipeline hazards and their Resolution Mechanisms like data forwarding, Delayed Branch, Branch Prediction, Dynamic Branch Prediction, Concept of Vector processing.

UNIT – IV (12 Hours)

Instruction Level Parallelism (ILP) Instruction-level Parallelism: Introduction, Challenges, Limitations, Basic Compiler Techniques for ILP; Branch Prediction, Out of order execution, Dynamic Scheduling, Limitations of ILP. Introduction to Thread Level Parallelism (TLP) and Data Level Parallelism (DLP). Introduction to Virtualisation Architecture, Virtualisation as a concept of Cloud Computing.

**Practical component (if any) – Advance Computer System Architecture
(FPGA/Virtual Lab/Tejas Architecture Simulator)**

LIST OF PRACTICALS (Total Practical Hours – 30 Hours)

1. To design a 4-bit common bus using 4:1 mux to transfer data from register to bus.
2. To design a 2-bit combinational shifter circuit which implements the logical shift, circular shift, arithmetic shift for both direction.
3. To design 2 bit arithmetic circuit which performs the following arithmetic operations add, add with carry, subtract, subtract with borrow, increment and decrement.
4. Design of Arithmetic Logical Unit ALU
5. Design of Memory: Design of a RAM cell
6. Design of Memory: Design of a 4X4 RAM
7. Design of Direct Mapped Cache
8. Design of Associative Cache
9. Using Architectural Simulator Tejas as
 - a. Emulator
 - b. Transfer Engine

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- c. Translational Modules
- d. Micro architectural Simulation

Note: Students shall sincerely work towards completing all the above listed practicals for this course. In any circumstance, the completed number of practicals shall not be less than eight, experiment no. 9 is compulsory.

Essential/recommended readings

1. "Computer Architecture: A Quantitative Approach", by John L. Hennessy and David A. Patterson, Morgan Kaufmann, 5th edition, 2011, ISBN: 9780123838728.
2. "Computer System Architecture" by M. Morris Mano (Pearson Publication)

Suggestive readings

1. "Computer Organization and Architecture", William Stallings, Prentice Hall, 10th edition, 2015, ISBN-10: 013293633X, ISBN-13: 978-0132936330
2. "Advanced computer architecture", Kai Hwang, TMH. 2000

Note: Examination scheme and mode shall be as prescribed by the Examination Branch, University of Delhi, from time to time.